74LVT16244B; 74LVTH16244B

3.3 V 16-bit buffer/driver; 3-state

Rev. 05 — 21 March 2006 Product data sheet

1. General description

The 74LVT16244B; 74LVTH16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

2. Features

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 833 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

3. Quick reference data

Table 1. Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay nAn to nYn	C_L = 50 pF; V_{CC} = 3.3 V	-	1.8	-	ns
t_{PHL}	HIGH-to-LOW propagation delay nAn to nYn	C_L = 50 pF; V_{CC} = 3.3 V	-	1.7	-	ns
C_i	input capacitance	V_I = 0 V or 3.0 V	-	3	-	pF
C_o	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	9	-	pF
I_{CC}	quiescent supply current	outputs disabled; V_{CC} = 3.6 V; I_O = 0 A; V_I = GND or V_{CC}	-	70	-	µA

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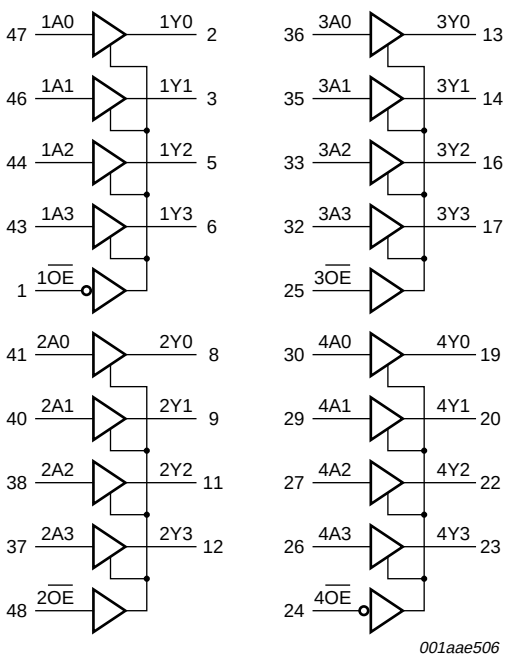
4. Ordering information

Table 2. Ordering information

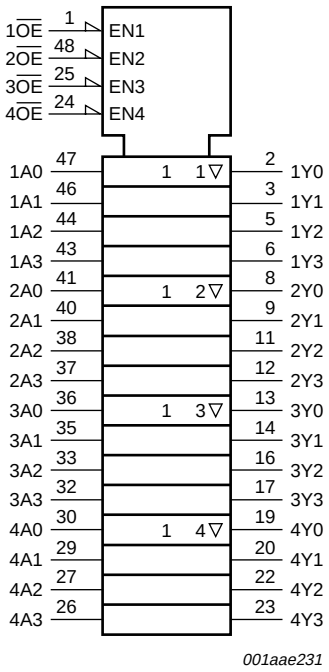
Type number	Package			
	Temperature range	Name	Description	Version
74LVT16244BDL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVT16244BDGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVT16244BEV	–40 °C to +85 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74LVTH16244BDL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVTH16244BDGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

5. Functional diagram



Pin numbers are shown for SSOP and TSSOP packages only.

Fig 1. Logic symbol



Pin numbers are shown for SSOP and TSSOP packages only.

Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

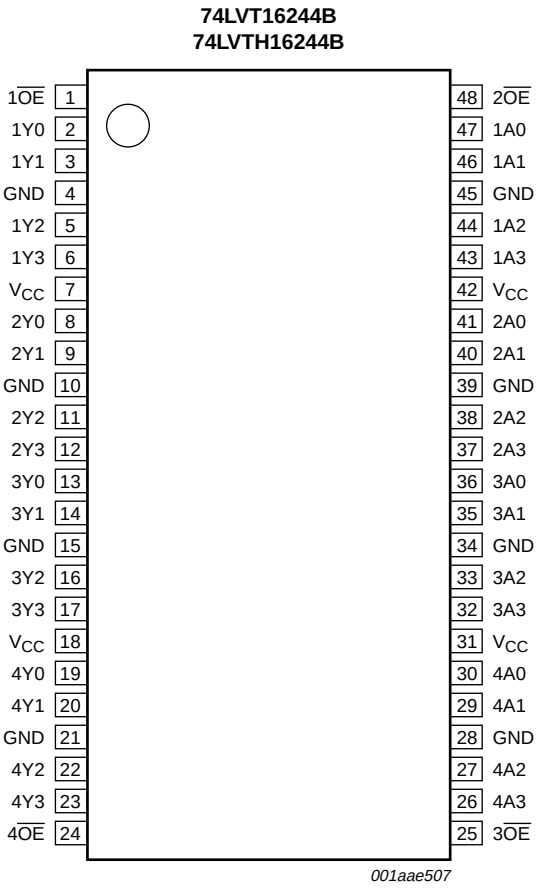
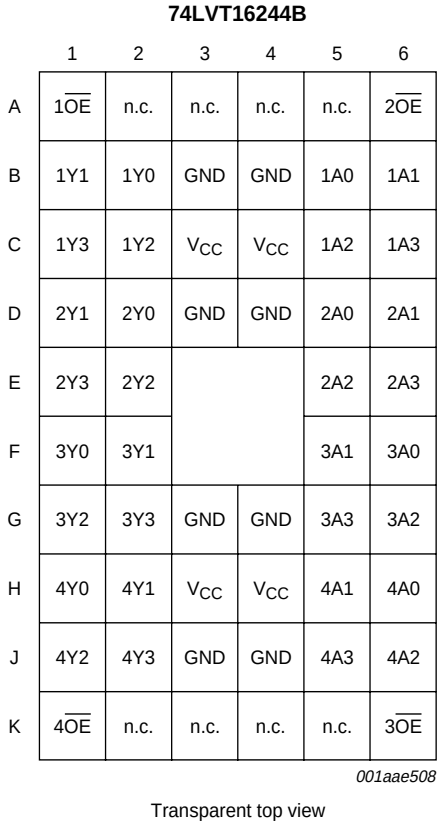


Fig 3. Pin configuration for SSOP48 and TSSOP48



Transparent top view

Fig 4. Pin configuration for VFBGA56

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
$1\overline{OE}$	1	A1	output enable input $1\overline{OE}$
n.c.	-	A2, A3, A4, A5	not connected
1Y0	2	B2	data output 1Y0
1Y1	3	B1	data output 1Y1
GND	4	B3	ground (0 V)
1Y2	5	C2	data output 1Y2
1Y3	6	C1	data output 1Y3
V_{CC}	7	C3	supply voltage
2Y0	8	D2	data output 2Y0

Table 3. Pin description *...continued*

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
2Y1	9	D1	data output 2Y1
GND	10	D3	ground (0 V)
2Y2	11	E2	data output 2Y2
2Y3	12	E1	data output 2Y3
3Y0	13	F1	data output 3Y0
3Y1	14	F2	data output 3Y1
GND	15	G3	ground (0 V)
3Y2	16	G1	data output 3Y2
3Y3	17	G2	data output 3Y3
V_{CC}	18	H3	supply voltage
4Y0	19	H1	data output 4Y0
4Y1	20	H2	data output 4Y1
GND	21	J3	ground (0 V)
4Y2	22	J1	data output 4Y2
4Y3	23	J2	data output 4Y3
$4\overline{OE}$	24	K1	output enable input $4\overline{OE}$
n.c.	-	K2, K3, K4, K5	not connected
$3\overline{OE}$	25	K6	output enable input $3\overline{OE}$
4A3	26	J5	data input 4A3
4A2	27	J6	data input 4A2
GND	28	J4	ground (0 V)
4A1	29	H5	data input 4A1
4A0	30	H6	data input 4A0
V_{CC}	31	H4	supply voltage
3A3	32	G5	data input 3A3
3A2	33	G6	data input 3A2
GND	34	G4	ground (0 V)
3A1	35	F5	data input 3A1
3A0	36	F6	data input 3A0
2A3	37	E6	data input 2A3
2A2	38	E5	data input 2A2
GND	39	D4	ground (0 V)
2A1	40	D6	data input 2A1
2A0	41	D5	data input 2A0
V_{CC}	42	C4	supply voltage
1A3	43	C6	data input 1A3
1A2	44	C5	data input 1A2
GND	45	B4	ground (0 V)

Table 3. Pin description *…continued*

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
1A1	46	B6	data input 1A1
1A0	47	B5	data input 1A0
$2\overline{OE}$	48	A6	output enable input $2\overline{OE}$

7. Functional description

7.1 Function table

Table 4. Function table[1]

Control	Input	Output
$n\overline{OE}$	nAn	nYn
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	–64	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
I_{OH}	HIGH-state output current		-	-	–32	mA
I_{OL}	LOW-state output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C[1]							
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		-	–0.85	–1.2	V
V_{OH}	HIGH-state output voltage	I_{OH} = –100 µA; V_{CC} = 2.7 V to 3.6 V		V_{CC} – 0.2	V_{CC}	-	V
		I_{OH} = –8 mA; V_{CC} = 2.7 V		2.4	2.5	-	V
		I_{OH} = –32 mA; V_{CC} = 3.0 V		2.0	2.3	-	V
V_{OL}	LOW-state output voltage	V_{CC} = 2.7 V					
		I_{OL} = 100 µA		-	0.07	0.2	V
		I_{OL} = 24 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V					
		I_{OL} = 16 mA		-	0.25	0.4	V
		I_{OL} = 32 mA		-	0.3	0.5	V
		I_{OL} = 64 mA		-	0.4	0.55	V
I_{LI}	input leakage current						
	all input pins	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	0.4	10	µA
	control pins	V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	0.1	±1.0	µA
	data pins	V_{CC} = 3.6 V	[2]				
		V_I = V_{CC}		-	0.1	1	µA
		V_I = 0 V		-	–0.4	–5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	0.1	±100	µA

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{HOLD}	bus hold current data input	V_{CC} = 3 V	[3]				
		V_I = 0.8 V		75	135	-	µA
		V_I = 2.0 V		–75	–135	-	µA
		V_{CC} = 0 V to 3.6 V					
		V_I = 3.6 V		±500	-	-	µA
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V; V_{CC} = 3.0 V		-	50	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care	[4]	-	1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}					
		output HIGH: V_O = 3.0 V		-	0.5	5	µA
		output LOW: V_O = 0.5 V		-	+0.5	–5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		output HIGH		-	0.07	0.12	mA
		output LOW		-	4.0	6.0	mA
		outputs disabled	[5]	-	0.07	0.12	mA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input at V_{CC} – 0.6 V and other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_i	input capacitance	V_I = 0 V or 3.0 V		-	3	-	pF
C_o	output capacitance	outputs disabled; V_O = 0 V or 3.0 V		-	9	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C[1]						
t_{PLH}	LOW-to-HIGH propagation delay nAn to nYn	see Figure 5				
		V_{CC} = 2.7 V	-	-	4.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	1.8	3.2	ns
t_{PHL}	HIGH-to-LOW propagation delay nAn to nYn	see Figure 5				
		V_{CC} = 2.7 V	-	-	4.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	1.7	3.2	ns

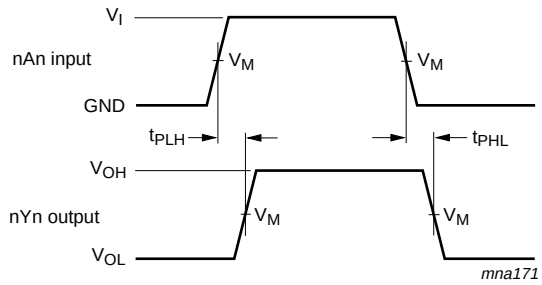
Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}	output enable time to HIGH-level	see Figure 6				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t_{PZL}	output enable time to LOW-level	see Figure 6				
		V_{CC} = 2.7 V	-	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.1	4.0	ns
t_{PHZ}	output disable time from HIGH-level	see Figure 6				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.5	ns
t_{PLZ}	output disable time from LOW-level	see Figure 6				
		V_{CC} = 2.7 V	-	-	4.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.9	4.0	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

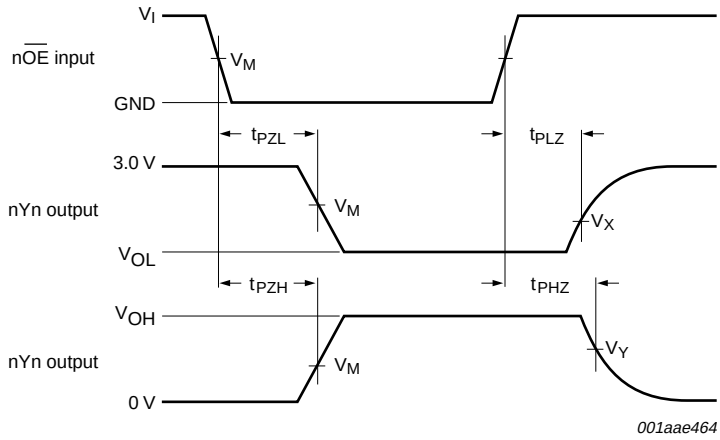
12. Waveforms



Measurements points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. Propagation delay input (nAn) to output (nYn)



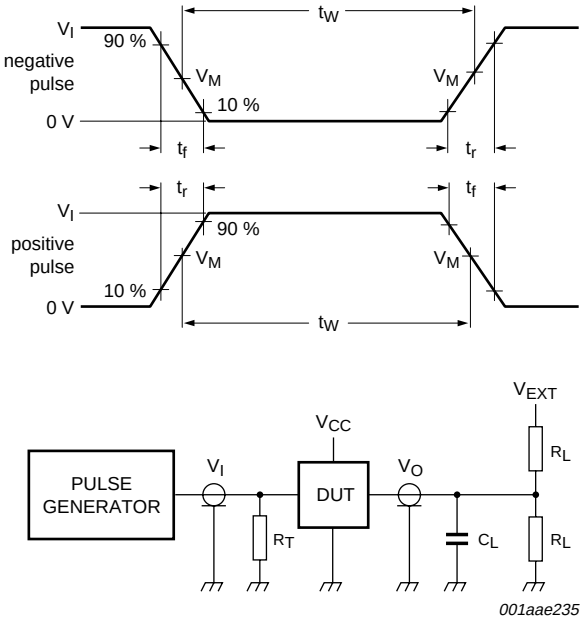
Measurements points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. 3-state output enable and disable times

Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

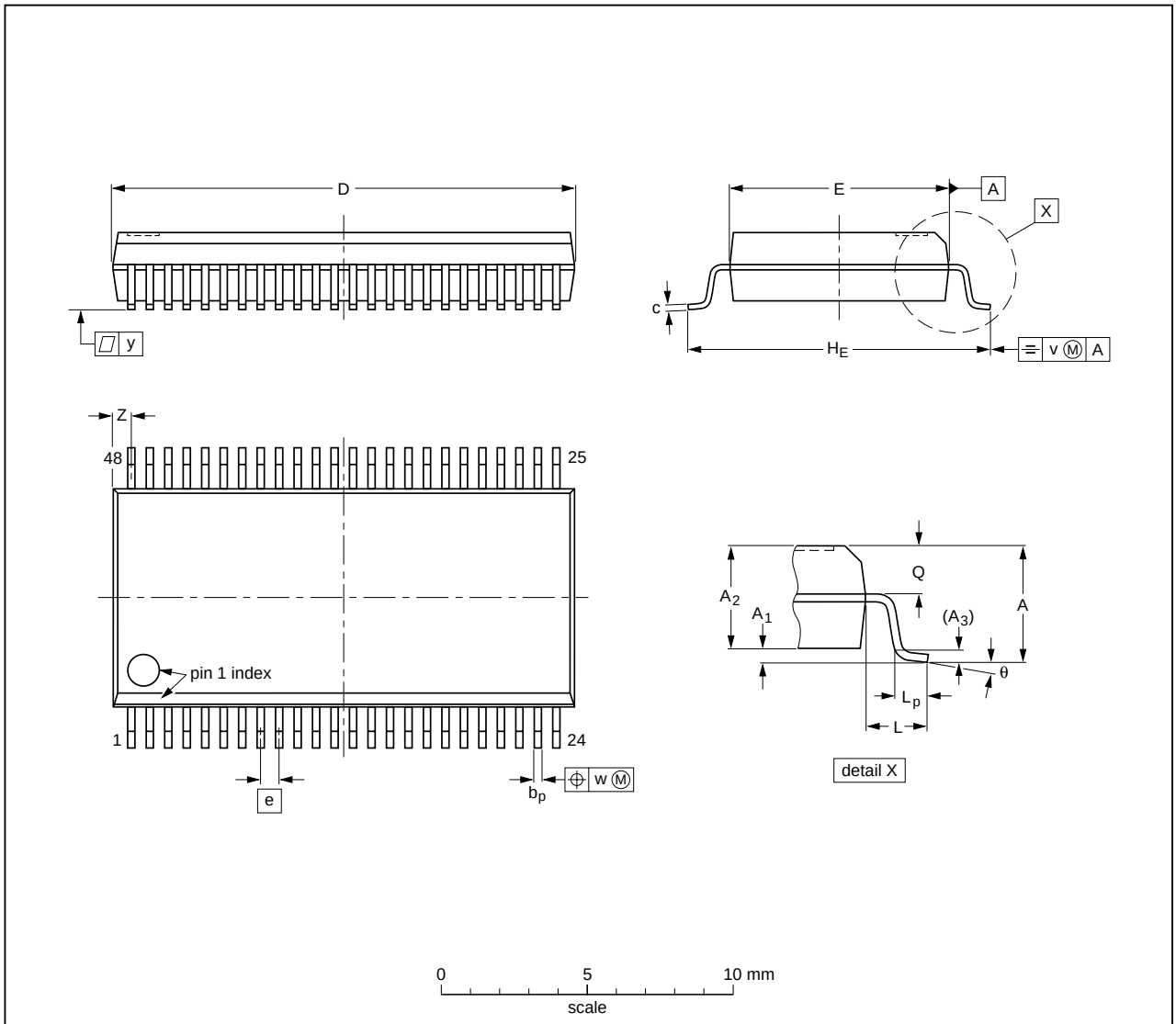
Fig 7. Load circuitry for switching times

Table 10. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

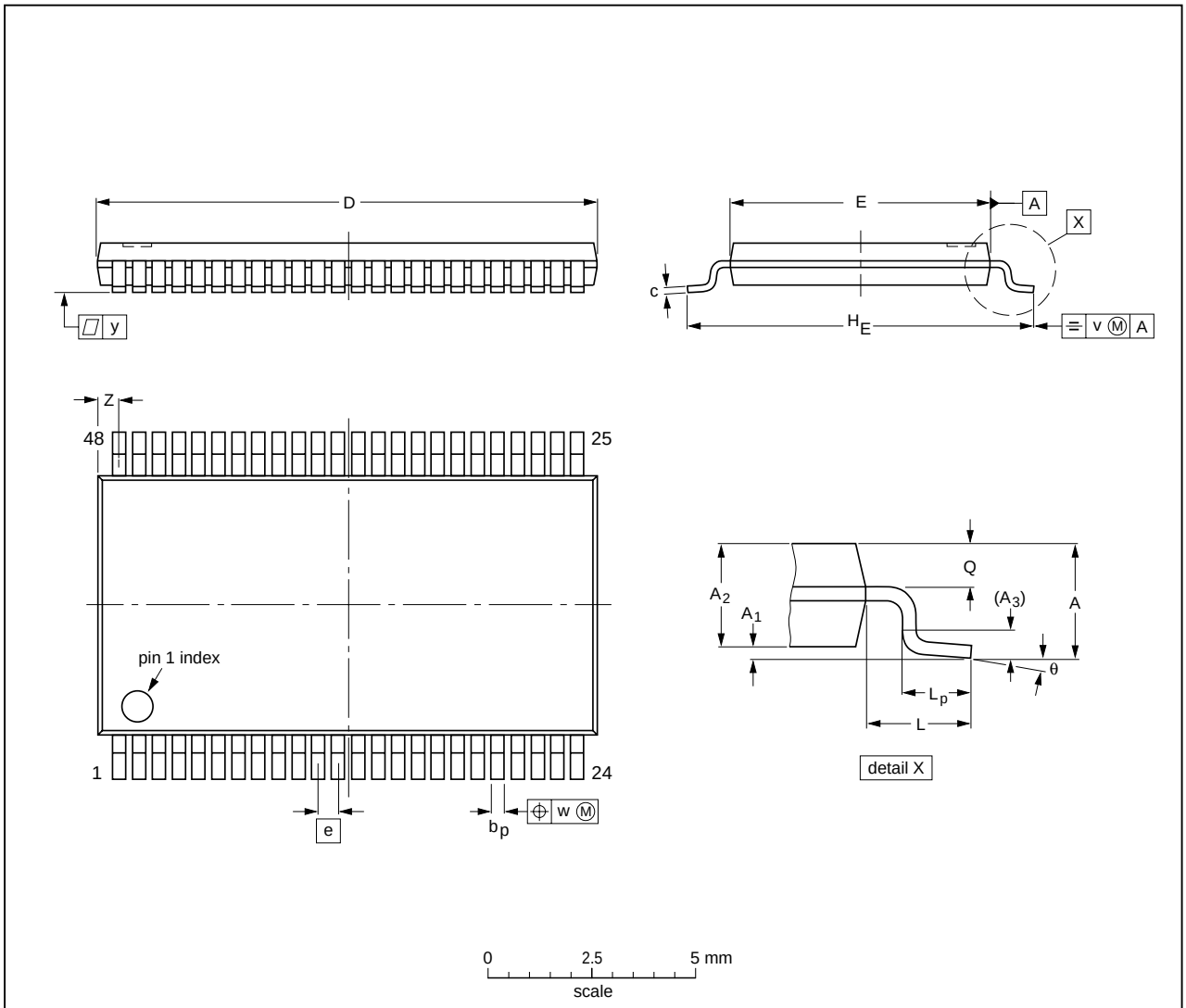
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

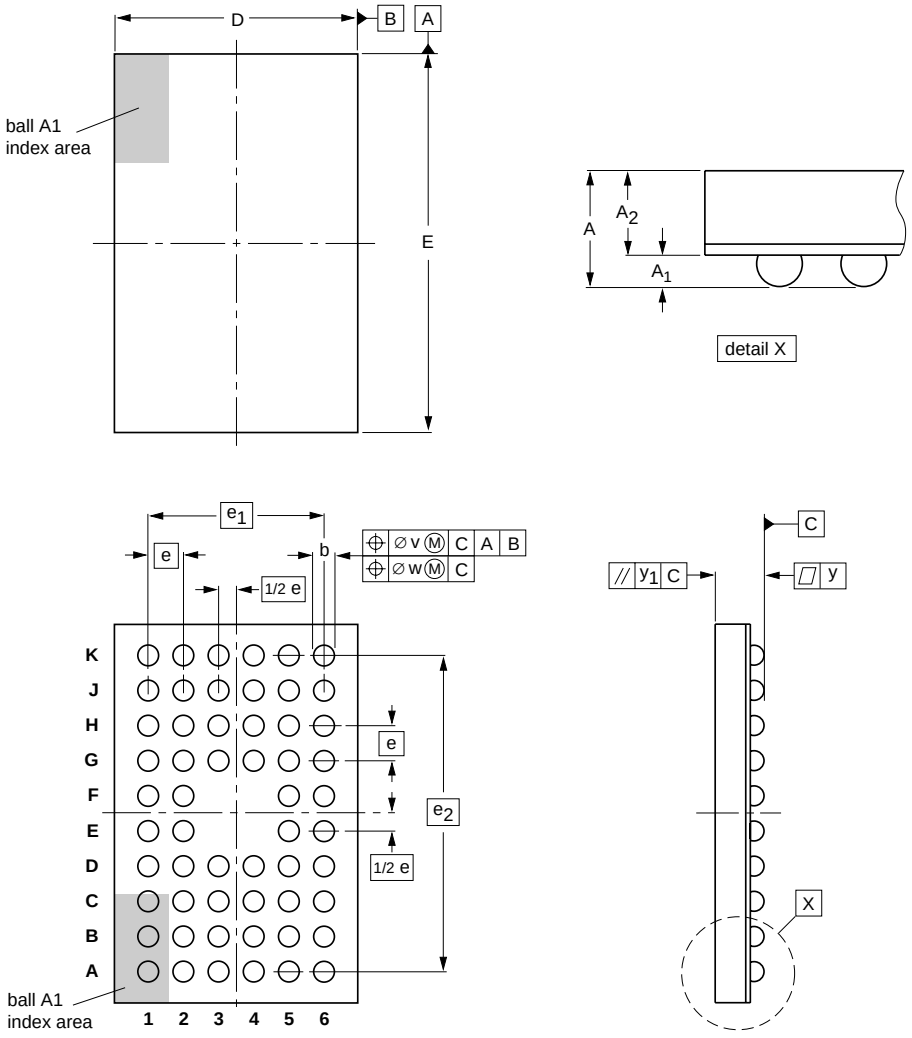
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1

0 2.5 5 mm

scale

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~02-08-08~~ 03-07-01

Fig 10. Package outline SOT702-1 (VFBGA56)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	Electrostatic Discharge
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH16244B_5	20060321	Product data sheet	-	74LVT16244B_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 4: added type numbers 74LVTH16244BDL and 74LVTH16244BDGG.			
74LVT16244B_4	20021031	Product specification	-	74LVT16244B_3
74LVT16244B_3	19981007	Product specification	-	74LVT16244B_2
74LVT16244B_2	19980219	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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